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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,985	12/30/2003	Toru Takeuchi	TX-36203	8246
23494	7590	09/20/2006	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			KAPADIA, VARSHA A	
P O BOX 655474, M/S 3999			ART UNIT	
DALLAS, TX 75265			PAPER NUMBER	
			2627	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

This office action is responsive to the amendment filed on July 5, 2006.

Claims 1-21 are pending.

Rejection Under 35 U.S.C. 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klaassen et al (6,606,212) in view of Contreras et al (6,420,910).

With regards to claims 1 and 15, Klaassen et al disclose a current-sense bias circuit for use with a magnetoresistive (referred to as MR hereon) head (see figs. 3, 7-8 and disclosure thereof), comprising:

A voltage biasing portion configured to provide a bias voltage across the MR head (see col.9 lines 36-col.10 lines 26 and figs. 7-8 and disclosure thereof); and a current sensing portion coupled to the voltage biasing portion and configured to sense change in the bias current based on the resistivity change of the MR head (See fig. 3, 7-8 and disclosure thereof and col.10 line 3-17). As further recited in claim 15, Klaassen et al discloses a hard disk drive comprising a motor and a storage medium as recited in the claim (see fig.13 and disclosure thereof).

Klaassen et al fail to further disclose that the bias current subtracts the current from a first current path to a supply voltage node and adds current to a second current path to the supply voltage node as claimed.

Contreras et al. however, disclose such a current control capability based on a resistivity change as claimed. (see 3A, 3B 6 disclosure thereof and col.5 lines 24-60 and cols 6 lines 38-60).

It would have been obvious to one of ordinary skill in the art at the time this invention was made to modify the current sense bias circuit disclosed by Klassen et al with the above teaching of current control capability disclosed by Contreras et al in order to provide an apparatus/method including bias current subtracts the current from a first current path to a supply voltage node and adds current to a second current path to the supply voltage node based on the resistivity change of the MR head and hence to adjust/control the impedance.

With regards to claims 2 and 16, Klaassen et al disclose that the bias voltage is provided by first and second bipolar transistors (see fig. 3 elements 304-305, and bipolar transistors in fig. 7-8 and disclosure thereof).

With regards to claims 3 and 17, Klaassen disclose that the MR head interposes first and second emitters of the bipolar transistors (see fig.7 elements 704,704', 701; fig.8 elements 801, 804,804',804'' and disclosure thereof).

With regards to claims 4 and 18, Klaassen disclose that the source for the bias voltage interposes first and second bases of the bipolar transistors (see bias voltage and bipolar transistors in figs. 3, 7 and 8 and disclosure thereof).

With regards to claims 5 and 19, Klaassen disclose that the change in the bias current employs first and second current sources (see current sources in figs. 7-8 and disclosure thereof).

With regards to claims 6 and 20, Klaassen disclose that the change in bias current provides a proportional differential voltage (see fig. 8 disclosure thereof and col.10 lines 3-18).

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With regards to claims 7 and 21, Klaassen disclose that the first and second resistors are employed to develop the proportional differential voltage (See R1 and R2 in figs. 7-8 and disclosure thereof).

With regards to claims 8-14, the method recited in claims 8-14 corresponds to the apparatus recited in claims 1-7 and 15-21, respectively. Therefore the rejection applied to claims 1-7 and 15-21 is also applied to claims 8-14 for the same reasons of anticipation.

Response To Remarks

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Varsha A. Kapadia whose telephone number is (571) 272-7557. The examiner can normally be reached on Mon Tue and Thurs. from 6:30 AM to 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea Wellington can be reached on 571 272 4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VK



ANDREA WELLINGTON
SUPERVISORY PATENT EXAMINER

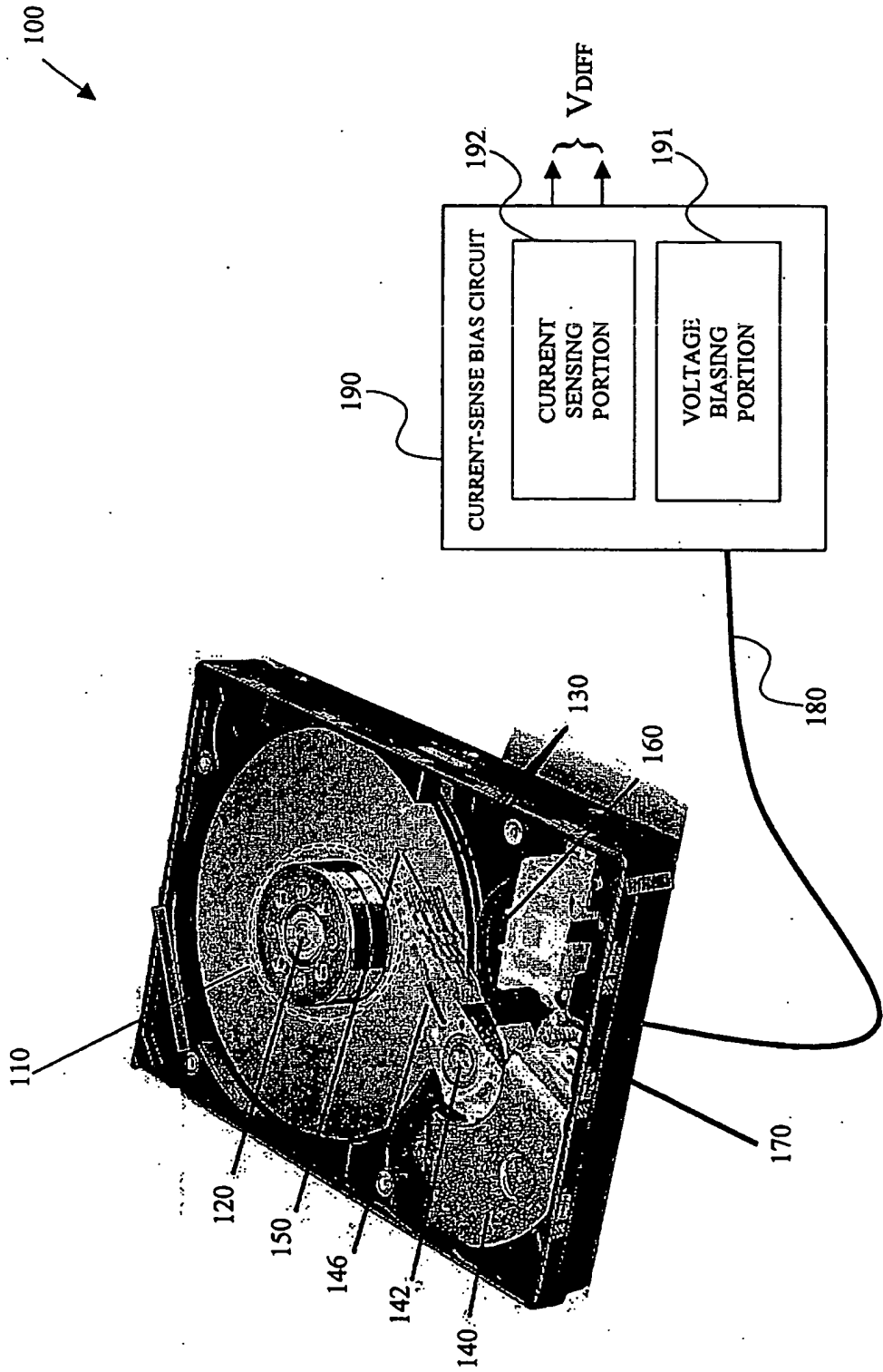
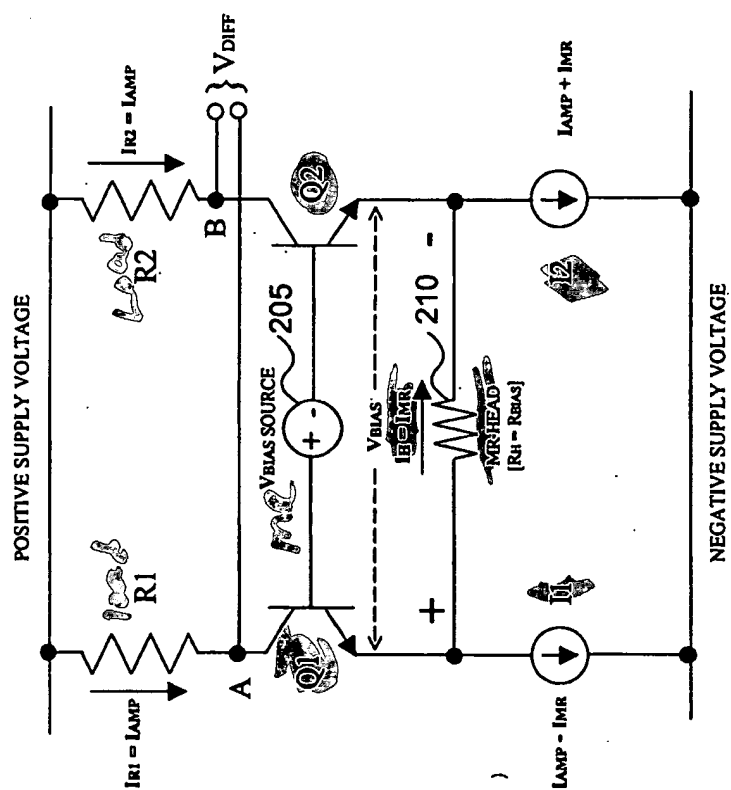


FIGURE 1

200



Trans

FIGURE 2

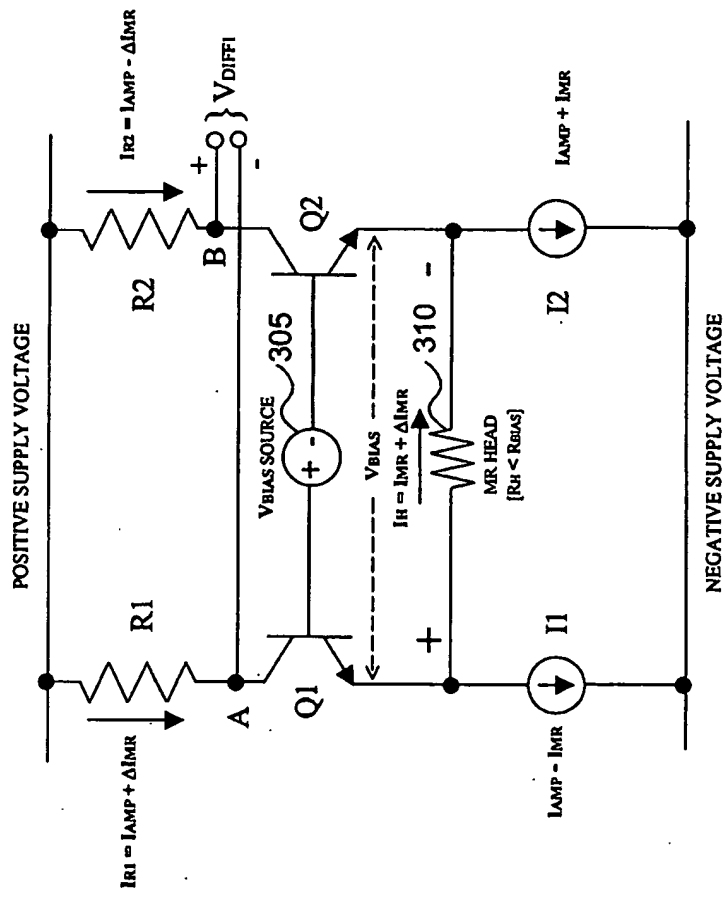


FIGURE 3

400

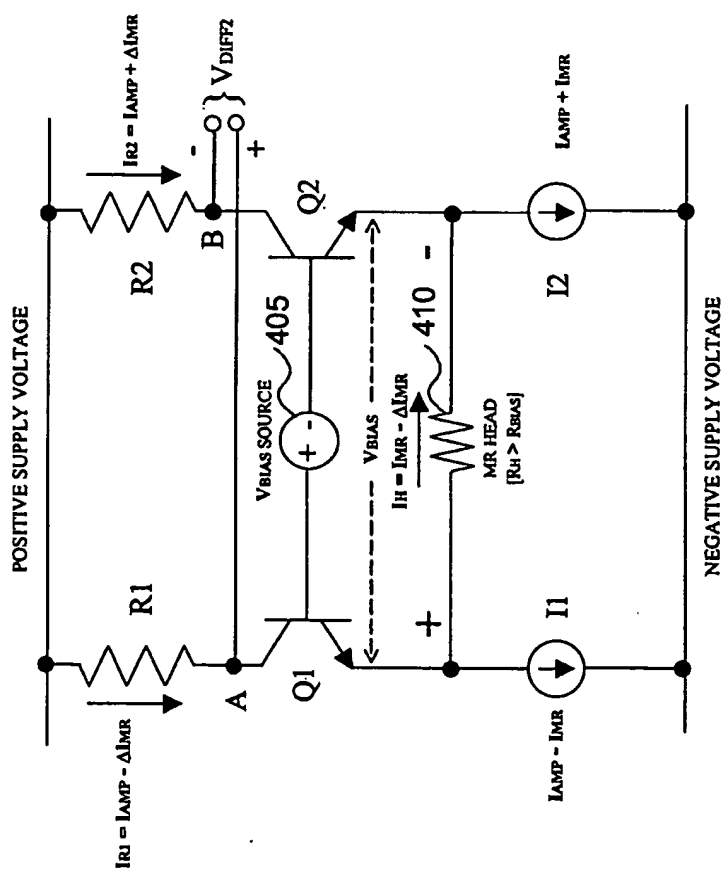


FIGURE 4

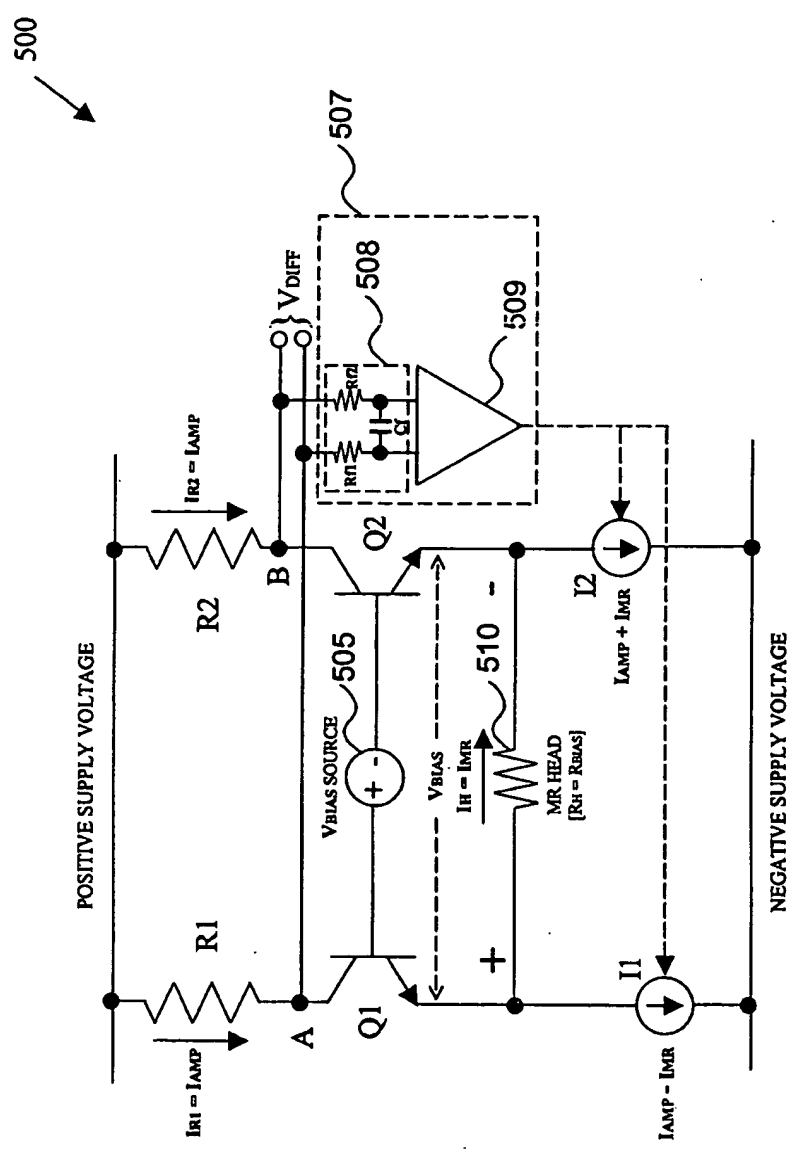


FIGURE 5

600

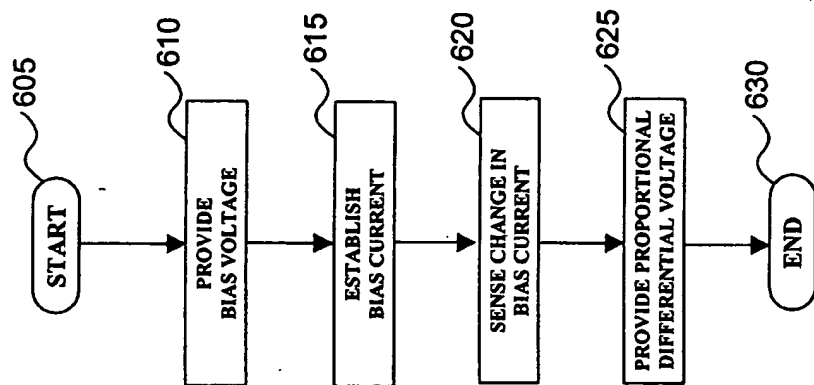


FIGURE 6